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GLAST LAT Calorimeter
Front-End Electronics (GCFE) ASIC

Chip 4.3 Development Functional Test Report

January 30, 2002

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Change History Log

Revision	Effective Date	Description of Change

Table of Contents

List of Figures

Applicable Documents:

1. LAT-SS-XXXXX-D1, "GLAST Calorimeter Analog Front-End ASIC Development Test Procedure", Tammy Faulkner, January 30, 2002.

2. LAT-SS-00423-D4, "GLAST LAT Design Description of the GLAST Calorimeter Front-End Electronics (GCFE) ASIC (GCFE4 submission), W. Neil Johnson and James Ampe, November 28, 2001.

3. LAT-SS-00089-D2, "GLAST LAT GLAST Calorimeter Front-End Electronics (GCFE) ASIC Specification, W. Neil Johnson, January 10, 2001.

Test Description

This document gives the test results from the initial execution of the GCFE ASIC Development Test Procedure as documented in item 1 above. This test exercises the functionality and evaluates the performance of the ASIC chip. Where possible, the functionality of individual sub-devices on the ASIC are exercised and verified. Complete data acquisition sequences are performed to confirm end-to-end functionality and to verify those sub-devices that cannot be individually tested. Finally, Energy Range, Noise, and Linearity measurements are made as a measurement of performance.

This test does not perform a complete evaluation of specification compliance. That test is a separate procedure yet to be defined and executed.

The unit under test was GCFE ASIC 4.3. The testing was performed on NRL's GCFE test board S/N 1. All tests were performed with the nominally defined Pre-Amp Gain settings of LE = 5, HE = 13, unless otherwise stated. The complete test data and results can be found in the executed test procedure and accompanying spreadsheets. These spreadsheets will be kept on-file on the NRL network.

Test Summary:

All functionality of the ASIC chip under test was performed successfully with the following two exceptions:

- Chip Command Address Decoding: the current EGSE set-up does not allow verification of the chip command address decoding logic. This should be implemented in the near future.
- Fast Shaper and Trigger Verification: testing of this functionality was unsuccessful. For all FLE and FHE settings, the triggering appeared to be occurring from signal noise so that a high-rate, continuous trigger occurred even when no pulses were being injected. The triggering occurred so quickly that it often caused a lock-up of the test board I/O. Troubleshooting for problems with the test board is underway.

The following is a brief description of the results of each test:

- The Noise, and Linearity measurements were successfully made.

Figure 1: Evaluation of Range, Noise, and Linearity

	LEX8		**LEX1**		**HEX8**		**HEX1**	
	Expected	**Measured**	**Expected**	**Measured**	**Expected**	**Measured**	**Expected**	**Measured**
Threshold	2 MeV		5 MeV		100 MeV		300 MeV	
Upper Limit	200 MeV	184 MeV	1.6 GeV	1.3 GeV	12.8 GeV	1.18 GeV	100 GeV	8.84 GeV
Noise	0.4 MeV	1.8 MeV	0.4 MeV	6 MeV	2.5 MeV	11 MeV	2.5 MeV	30 MeV
Linearity	+/- 0.5 %	+/- 0.5 %	+/- 0.5 %	+/- 5%	+/- 0.5 %	+/- 0.4 %	+/- 0.5 %	+/- 0.5 %

  - The low threshold could not be measured without successful operation of the internal trigger.
  - The noise is significantly better than that observed for Version 3 of the chip, but still 4.5 – 12 times higher than specifications.
  - The linearity of the LEX8, HEX8, and HEX1 channels is within specifications. The LEX1 channel shows a definite deviation from linearity.
  - The Energy ranges of the LE channels are close to the design specifications. The HE ranges are more than a factor 10 low than the design specifications. The calculations used to convert from Volts to MeV is described in detail in Appendix A.
- Command and Read-Back Function was successfully verified for all implemented commands over their full range of commandability.
- Discriminators: The functionality of all discriminators was verified. Several variations from design with the discriminator DAC settings were noted.
  - The REF_DAC displayed two, 6-bit ranges. The first range had the designed resolution with only ½ the range. The second range had the full range at ½ the resolution. The signal noise on the REF_DAC measurements was negligible.

  - The LOG_ACPT_DAC displayed the same characteristic two, 6-bit ranges as the REF_DAC. The noise, i.e. range in which either a true or false was reported, was between 40-60 mV, much higher than the specification of 4.8 mV.
  - The RNG_ULD_DAC also displayed the two 6-bit ranges. All three range discriminators showed lower transition values than designed, with the LEX8 and HEX8 offset by 700 mV and the LEX1 transition offset 300 mV lower. Also, the slope of the LEX1 discriminator was lower than the LEX8, HEX8 and designed values. Since all 3 discriminators are using the same ADC, a variation in the discriminators appears to exist.

- The Auto-Range logic also performed differently than expected, as it seemed to exhibit a preference for the HEX8 channel over the more-sensitive LEX1 channel. This may cause the HEX8 channel to be selected over the LEX1 channel in the upper portion of the LEX1 range.
- Most of the Pre-Amp Gain settings were measured and compared well with the GCFE4 Design Description submission.
- No leakage between the HE and LE circuits were measured within the normal charge injection range of each input. Further measurements with a high signal charge in the LE input will be made to simulate the dual-sized detectors.

It should also be noted that during the middle of this testing, the ability to inject an external pulse into the HE signal input channel was damaged. It has not been conclusively determined that the damage is on the test board or within the ASIC, although within the chip is suspected at this time. This did not effect using the calibration source as an input, and therefore testing was successfully completed. Once the chip is unsoldered from the test board and testing of chip 4.4 is performed, conclusive determination of the location of the damage can be performed.

Detailed Test Report:

1. Command Function Verification:

All Digital Read/Write registers on the GCFE chip were successfully written to and read back from for the full-range of values

2. Reference Voltage Verification

The V_REF is selected in as Analog Output in two methods. The first method uses the config register 0 Overwrite function. The second method is to observe the Analog Output Signal without triggers occurring. Measurements of the full range and the REF_DAC were taken using the oscilloscope and compared to the design description. Both methods were compared and determined to give the same signal levels.

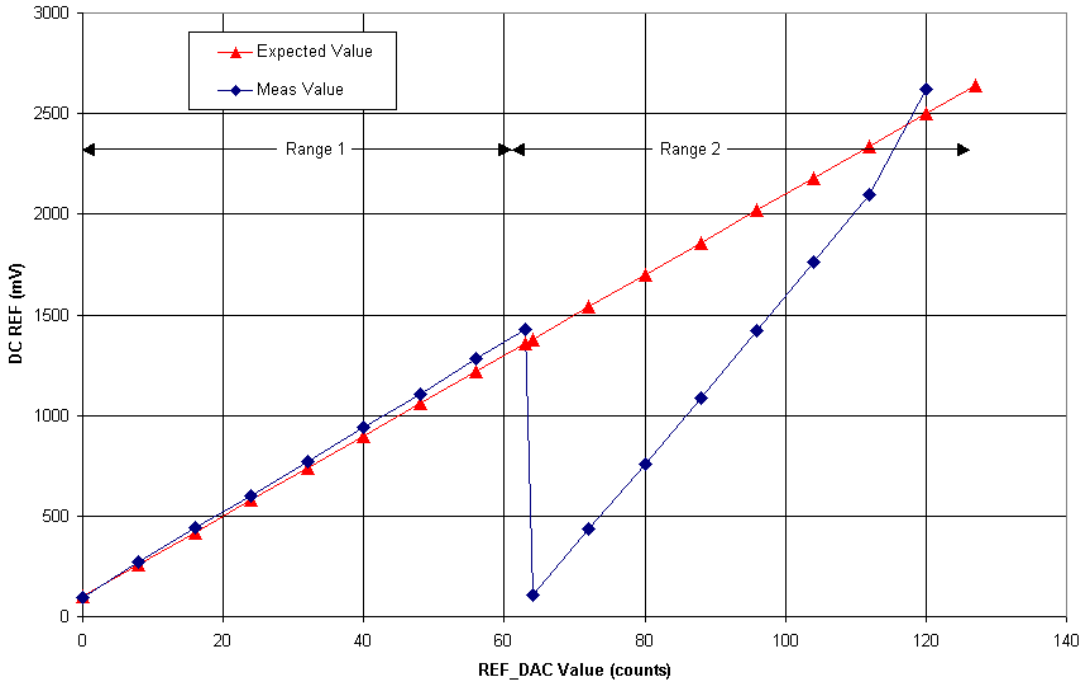
Figure 2: REF_DAC Measurements

	Expected	Measured	
		Range 1	Range 2
Low Limit of Range	100 mV	93.7 mV	110.3 mV
High Limit of Range	2640 mV	1426 mV	~2600 mV
Resolution	20 mV	21.07 mV	41.62 mV
Number of Bits	7	6, with 2 Ranges.	

Several differences with the design values were noted. First is that instead of a single 7-bit range, the REF_DAC is divided into two 6-bit ranges. The first range has the designed resolution but only half the range. When the DAC value exceeds 63 counts, the DC_REF wraps to the initial value for what I define as a second range. The second range has half the resolution of the first range and therefore covers the complete design range. The over-all result is that for the higher half of the range, the resolution is only half of design, and that commanding the V_REF over the full range is more complex.

The second observation is that the V_REF signal has a large ringing when the value exceeds 2.5 Volts. The ringing was so large that measurements above a DAC value of 120 were not attempted in fear of damaging the electronics.

Figure 3: REF_DAC Plot



3. Logic Accept Discriminator Verification

Functionality of the Logic Accept Discriminator was made along with measurements of the LOG_ACPT_DAC. Measurements were taken by plotting the Analog Output ADC values on a histogram with one symbol if the Logic Accept Discriminator indicated true, and another if it indicated False, see the figure below. The point where the two histograms meet was recorded as the LOG_ACPT threshold and the distance the histograms overlapped was recorded as the noise value. The values were compared with the concept design as follows.

The resulting measurements are shown in the graph below. Similar to the REF_DAC measurements, the LOG_ACPT discriminator is not the designed 7-bit but is actually (2) 6-bit ranges. Also notice that the logic accept discriminator noise is 20-68 mVolts.

Figure 4: Log Accept Discriminator Measurement

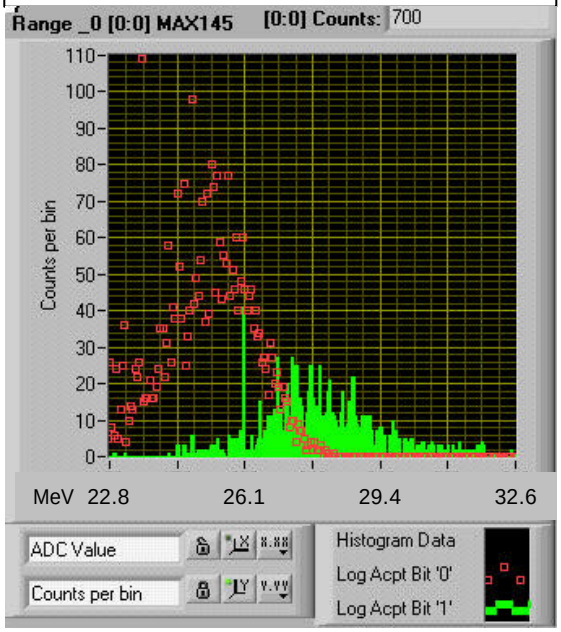


Figure 5: LOG_ACPT_DAC Plot

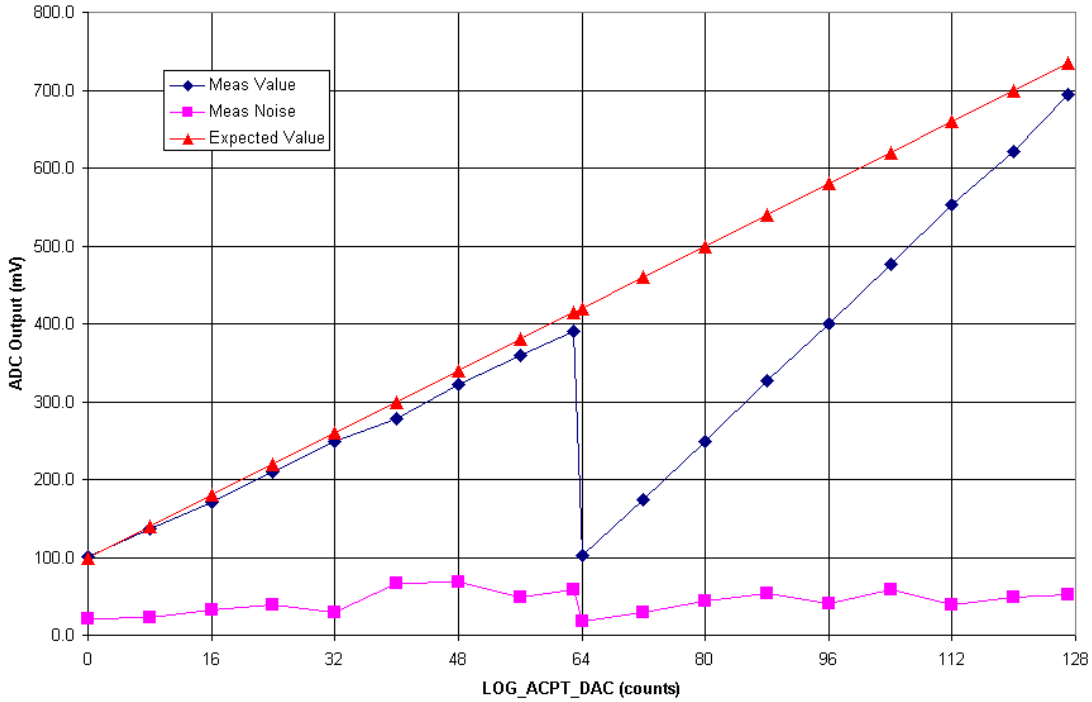


Figure 6: LOG_ACPT_DAC Measurements

	mV			MeV		
	Expected	Range1	Range2	Expected	Range1	Range2
Resolution:	**5**	**4.61**	**9.37**	**0.41**	**0.38**	**0.78**
Low Limit of Range:	**100**	**101**	**102**	**0**	**0.08**	**0.17**
High Limit of Range:	**735**	**390**	**694**	**53**	**24.2**	**49.6**
Noise	**4.8**	**42.9**	**42.5**	**0.4**	**3.58**	**3.55**

4. Auto-Range Functionality and Auto-Range Discriminator Verification

The functionality of the Auto-Range range determination was tested. It was determined to be functional, but not exactly as expected. It was the test engineer's belief that the Auto-Range logic started with LEX8 (the most sensitive channel) and progressed in order of sensitivity to the least sensitive range, choosing the range that is the most sensitive without exceeding the RNG_ULD_DISC level. By using 2 Pulse Generators to inject signals of different magnitudes into the LE and HE channels, it appears that the logic skips the LEX1 channel on its initial determination of best range and returns to it only if HEX8 is not saturated. With the assumption that HEX8 will never be saturated before LEX1, the functionality should be successful.

GCFE Ranges
- LEX8 most sensitive
- LEX1
- HEX8 ↓
- HEX1 least sensitive

The Auto-Range discriminator was then measured. Using the calibration strobe as in input and the following settings to have the auto-range choose the correct transitions did this.

Range 0 → 1 transition: LE Auto Range ENA, HE Auto Range DIS

Range 1 → 2 transition: HE Auto Range DIS, CALIB Gain 1, LE CAL ENA, and HE CAL DIS

Range 2 → 3 transition: LE Auto Range DIS, HE Auto Range ENA

The results are in the plot and table below.

Figure 7: RNG_ULD_DAC Plot

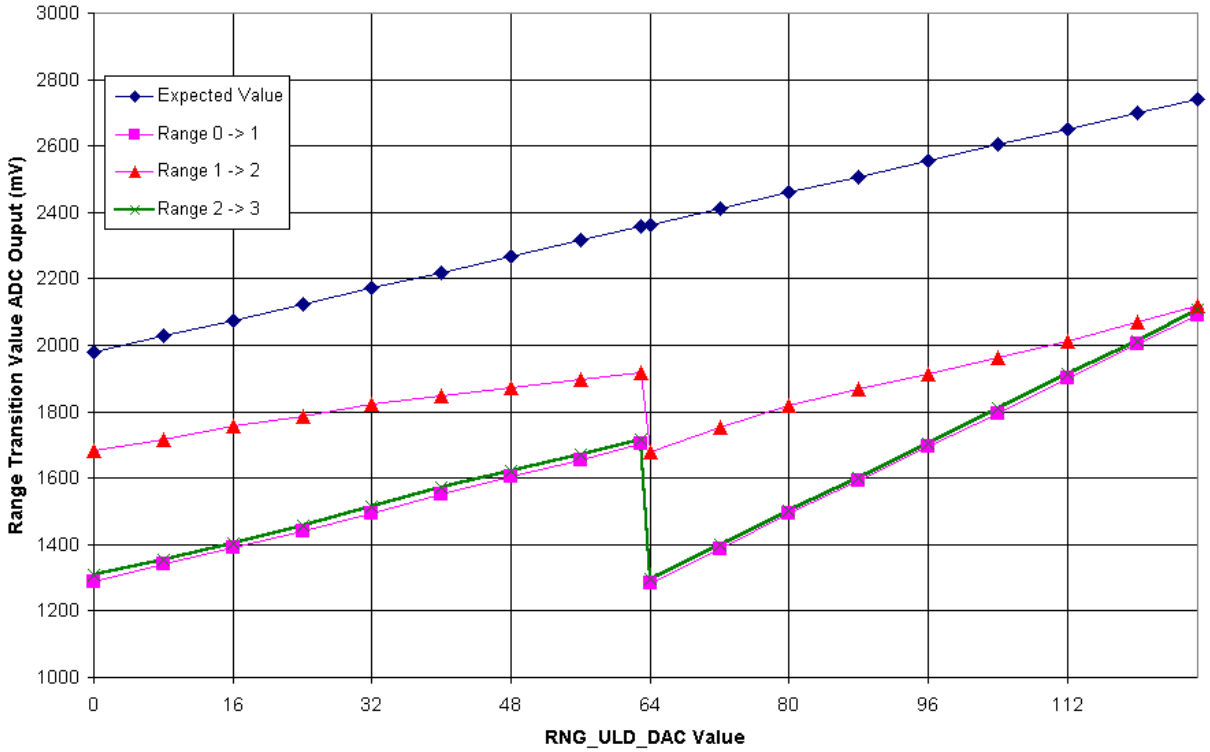


Figure 8: RNG_ULD_DAC Measurements (mV)

	Expected	Range 0 -> 1 Tran		Range 1 -> 2 Tran		Range 2 -> 3 Tran	
		Range 1	**Range 2**	**Range 1**	**Range 2**	**Range 1**	**Range 2**
Resolution	**6**	**6.59**	**12.81**	**3.70**	**6.74**	**6.57**	**12.85**
Low Limit of Range	**1980**	**1290**	**1285**	**1683**	**1678**	**1310**	**1295**
High Limit of Range	**2742**	**1704**	**2092**	**1917**	**2119**	**1718**	**2108**

Again, similar to the previous discriminator measurements, the discriminator has two 6-bit ranges with the slopes of the second range being nearly twice that of the first range. Unique to this discriminator is that the values are offset from the expected value and that not all three range transitions showed the same discriminator behavior for the same ADC setting.

5. Trigger Discriminator and Logic

Several attempts were made to test the functionality of the trigger capability of the ASIC. All attempts failed. Regardless of the FLE_DAC and FHE_DAC settings, when either of the trigger functions is enabled in Configuration Register 1, triggers occur continuously at a very high rate as if they are triggering off of high-frequency noise. Further trouble-shooting of the Fast-shaper output and possible problems with the test board are planned for the next few days to attempt to make these measurements.

6. Pre-Amp Gain Measurements

Measurements of the Analog Output values were made for most of the different Pre-Amp Gain configurations. The measurements were made using the CAL strobe as input with CAL Gain = 0 and stepping the CAL DAC over it's complete range of 0 – 1.25 Volts in 40 steps. The trigger came from the EGSE software so that low signal levels could be observed. The recorded measurement is the average of 40 ADC readings in each step.

Figure 9: Pre-Amp Gain Measurements

Slope of Pre-Amp Gain Selection when value is above threshold and un-saturated (< 2.2 Volts). All values are in Volts. The ratios are the Measured / Designed values.

	Pre-Amp Design Gain (Volts)	Meas ADC LEX8 (Volts)	Ratio M/D	Meas ADC LEX1 (Volts)	Ratio M/D	Pre-Amp Design Gain (Volts)	Meas ADC HEX8 (Volts)	Ratio M/D	Meas ADC HEX1 (Volts)	Ratio M/D
Gain0	4.41	6.33	1.43	0.95	0.215	15.24	21.12	1.39	2.86	0.188
Gain1	3.12	4.50	1.44	0.74	0.237	6.27	9.09	1.45	1.20	0.191
Gain2	2.42	3.53	1.46	0.59	0.243	3.95	5.75	1.45	0.76	0.192
Gain3	1.97	2.85	1.45	0.47	0.238	2.88				
Gain4	1.68	2.44	1.45	0.39	0.230	2.27	3.33	1.47	0.43	0.190
Gain5	1.45	2.12	1.46	0.32	0.220	1.87				
Gain6	1.28	1.85	1.44	0.27	0.209	1.59	2.36	1.48	0.29	0.185
Gain7	1.14	1.65	1.45	0.24	0.207	1.39				
Gain8						4.35	6.37	1.46	0.84	0.192
Gain9						3.09				
Gain10						2.40	3.52	1.47	0.45	0.189
Gain11						1.96				
Gain12						1.65	2.45	1.49	0.31	0.188
Gain13						1.43				
Gain14						1.26	1.86	1.48	0.23	0.185
Gain15						1.13	1.65	1.46	0.21	0.183

Figure 10: LEX8 Pre-Amp Gains Plot

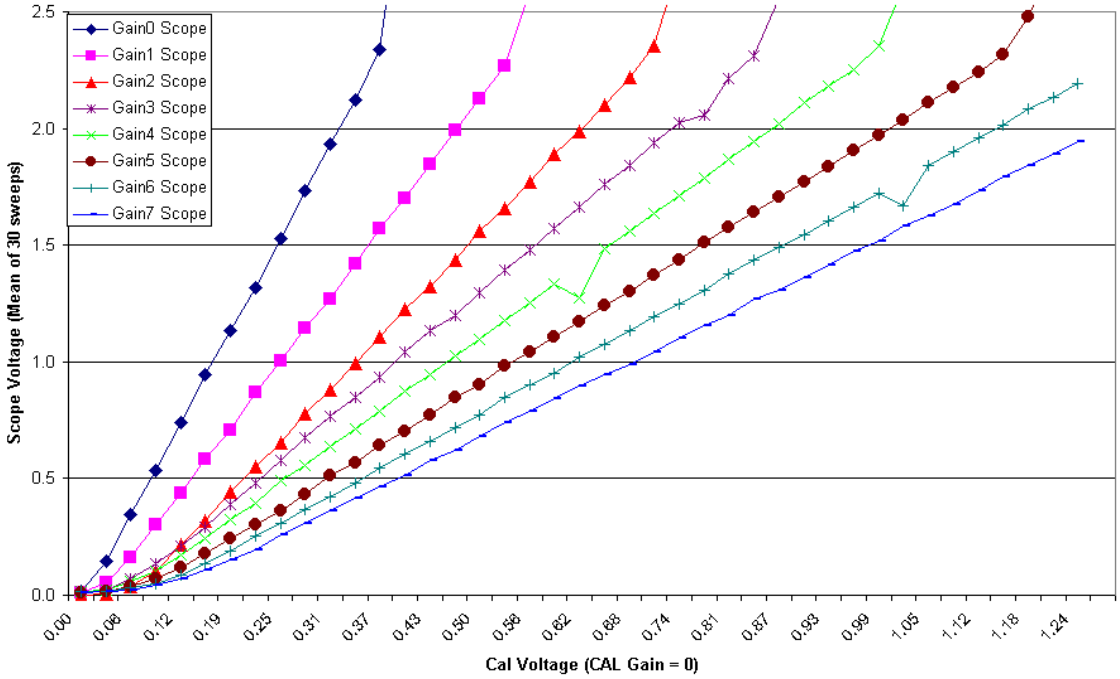


Figure 11: LEX1 Pre Amp Gains Plot

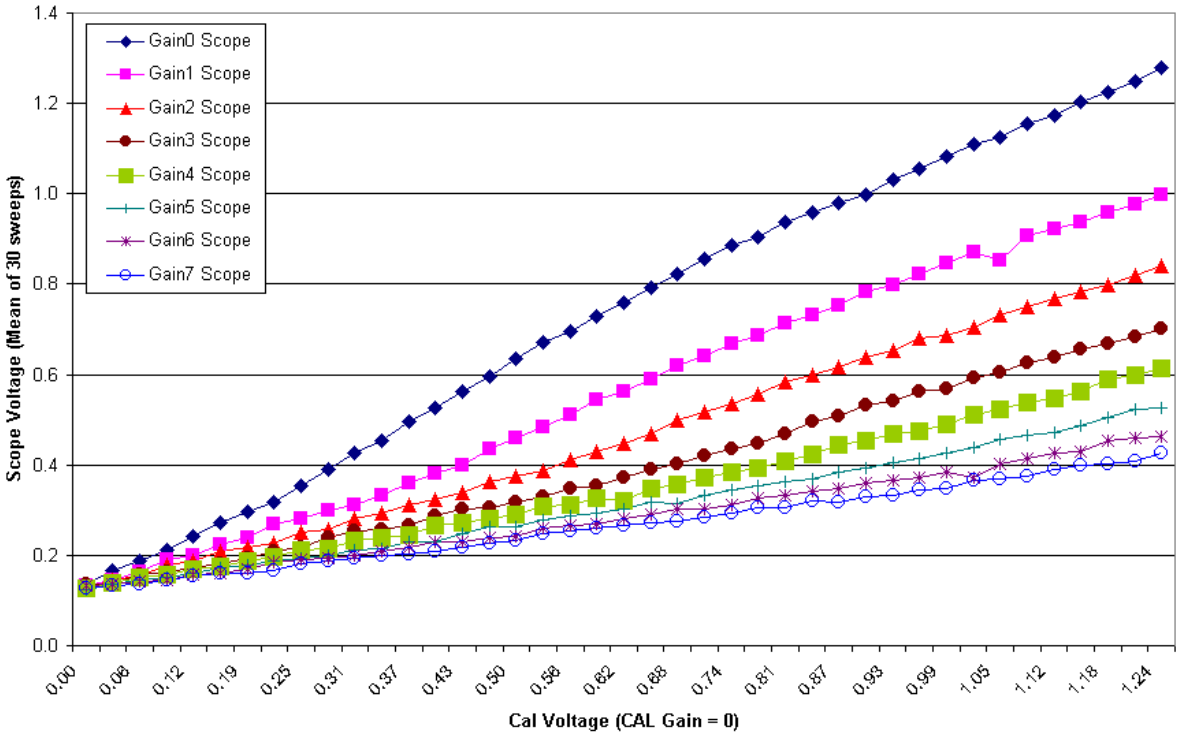


Figure 12: HEX8 Pre Amp Gains Plot

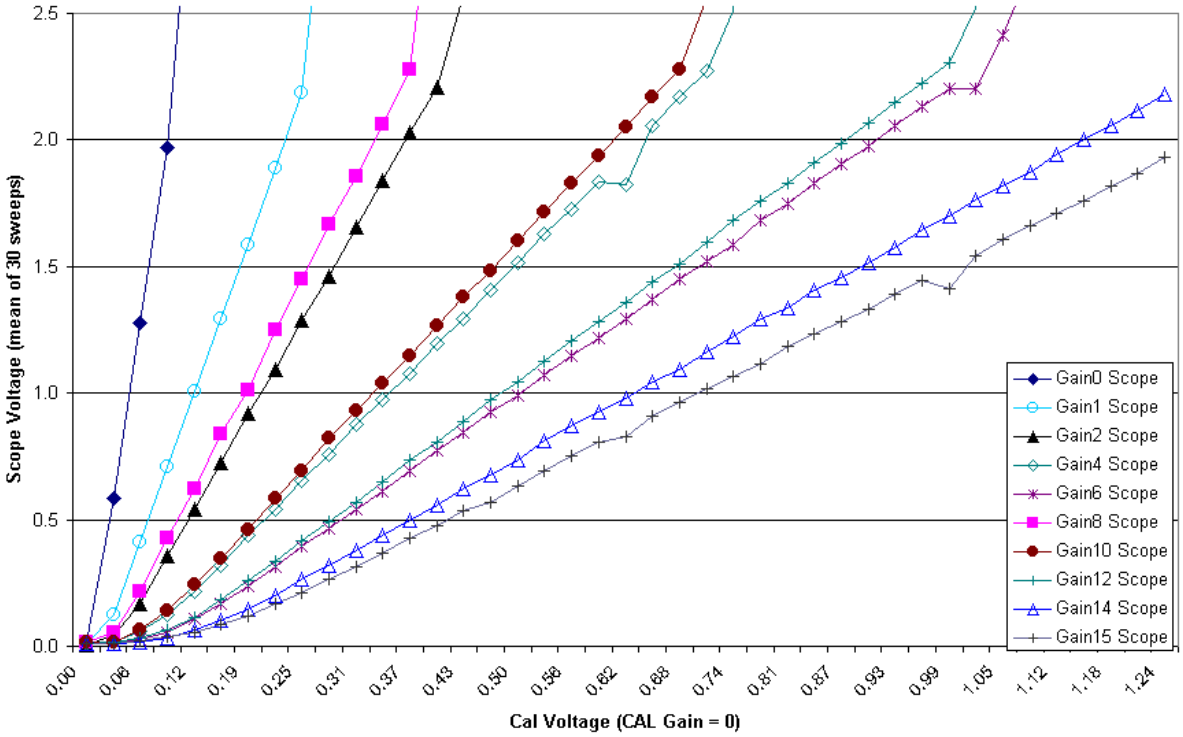
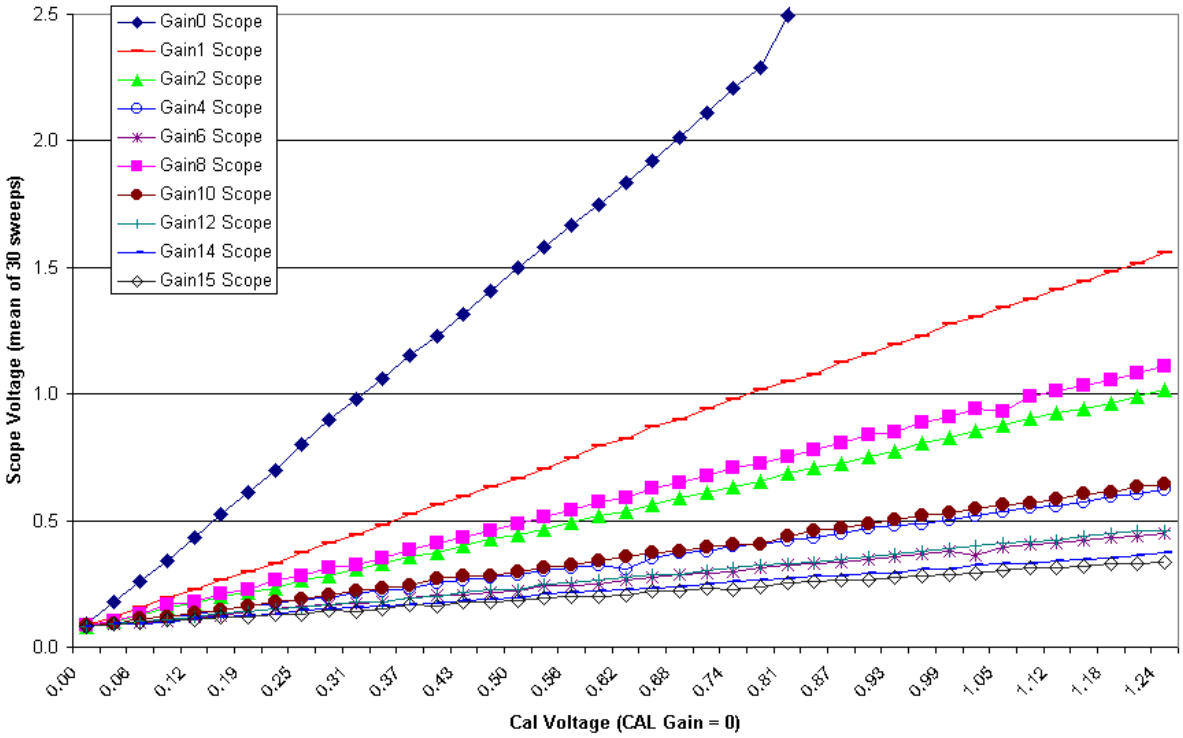


Figure 13: HEX1 Pre-Amp Gains Plot



7. Leakage between Channels

Measurements were made of the leakage between the HE channels and the LE channels by disabling the calibration for one and measuring all 4-channels analog output. The X8 channel measurements were done with CAL Gain = 0. The X1 channel measurements were done with CAL Gain – 1. The Pre-Amp gains were the nominal settings of LE=5, HE=13. The plots are shown below. There is no significant increase (< 0.5 mV) in the channels with their inputs disabled over the complete linear range of the enabled channel.

Figure 14: LE Signal leakage to HE Signal

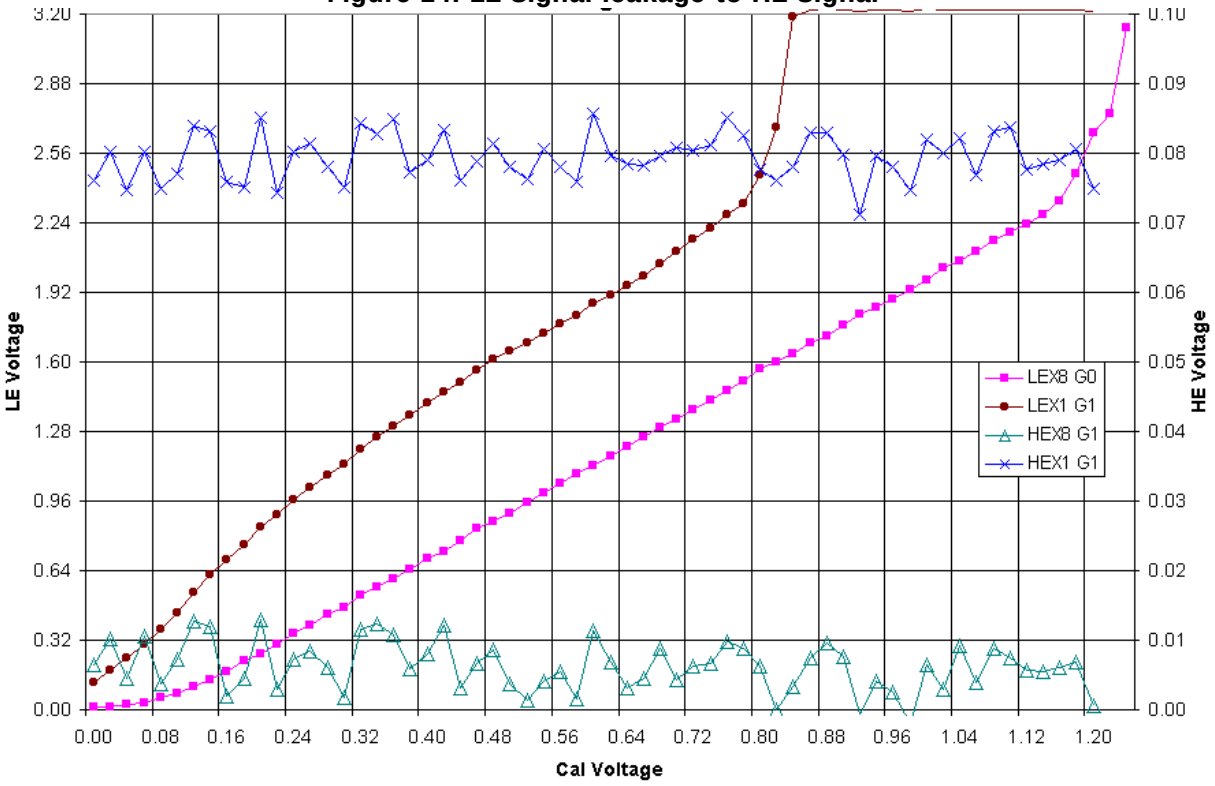
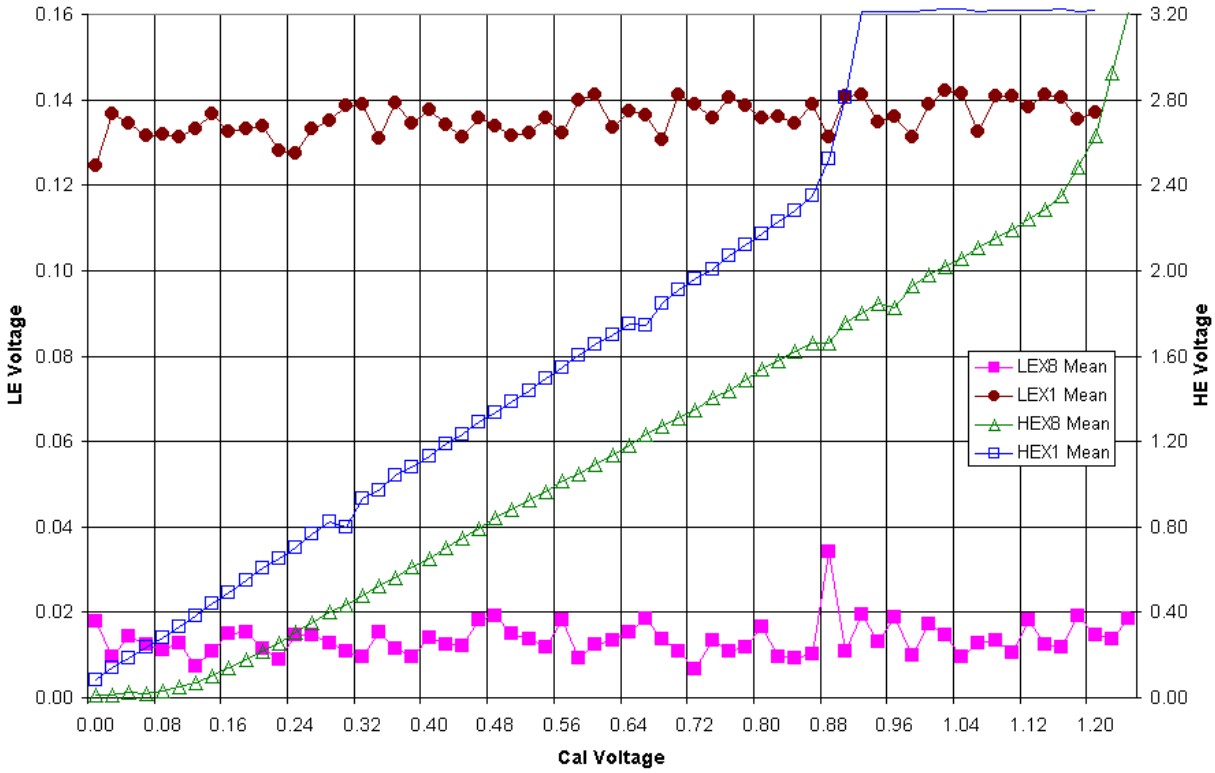


Figure 15: HE Signal leakage into LE Signal



8. Energy Range, Noise and Linearity

Energy range, noise and linearity measurements were taken several times in slightly different configurations. The data used in these plots were from the measurements taken on January 18, 2002, these measurements were made without the oscilloscope connected and with the signal input pins unsoldered and lifted from the test board. Identical measurements were made with the signal input pins soldered to the test board. No significant differences in either noise or linearity were seen between these two sets of measurements. The Pre-Amp Gain settings for all of these measurements were the nominal setting of LE=5 and HE=13.

Figure 16: Evaluation of Range, Noise, and Linearity

	LEX8		LEX1		HEX8		HEX1	
	Expected	**Measured**	**Expected**	**Measured**	**Expected**	**Measured**	**Expected**	**Measured**
Threshold	2 MeV		5 MeV		100 MeV		300 MeV	
Upper Limit	200 MeV	184 MeV	1.6 GeV	1.3 GeV	12.8 GeV	1.18 GeV	100 GeV	8.84 GeV
Noise	0.4 MeV	1.8 MeV	0.4 MeV	6 MeV	2.5 MeV	11 MeV	2.5 MeV	30 MeV
Linearity	+/- 0.5 %	+/- 0.5 %	+/- 0.5 %	+/- 5%	+/- 0.5 %	+/- 0.4 %	+/- 0.5 %	+/- 0.5 %

- Once internal triggering is successfully functioning, the threshold will be measured by determining the lowest possible trigger DAC setting that results in no triggers when pulses are not being injected. The calibration input will then be used to inject a signal.

The smallest calibration signal that results in 95% successful trigger rate will then be recorded as the threshold for that channel.

- Linearity is calculated for the measured Energy Range starting from the measured threshold (when available) until prior to saturation, which is determined when the noise on the signal increases dramatically at just over 2.2 Volts. Since the threshold measurements are not available, the linearity measurements started when the plot of Calibration Input to ADC Output showed an appearance of linearity. For the LEX1 and HEX1 channels, that was immediately. For the LEX8 channel, I started the linearity measurement at a Calibration Input value of 16.4 MeV. For the HEX8 channel, it was 115 MeV.
- These measurements were made using the software trigger so that low-energy values could be measured.

Figure 17: LEX8 Noise and Linearity Plot

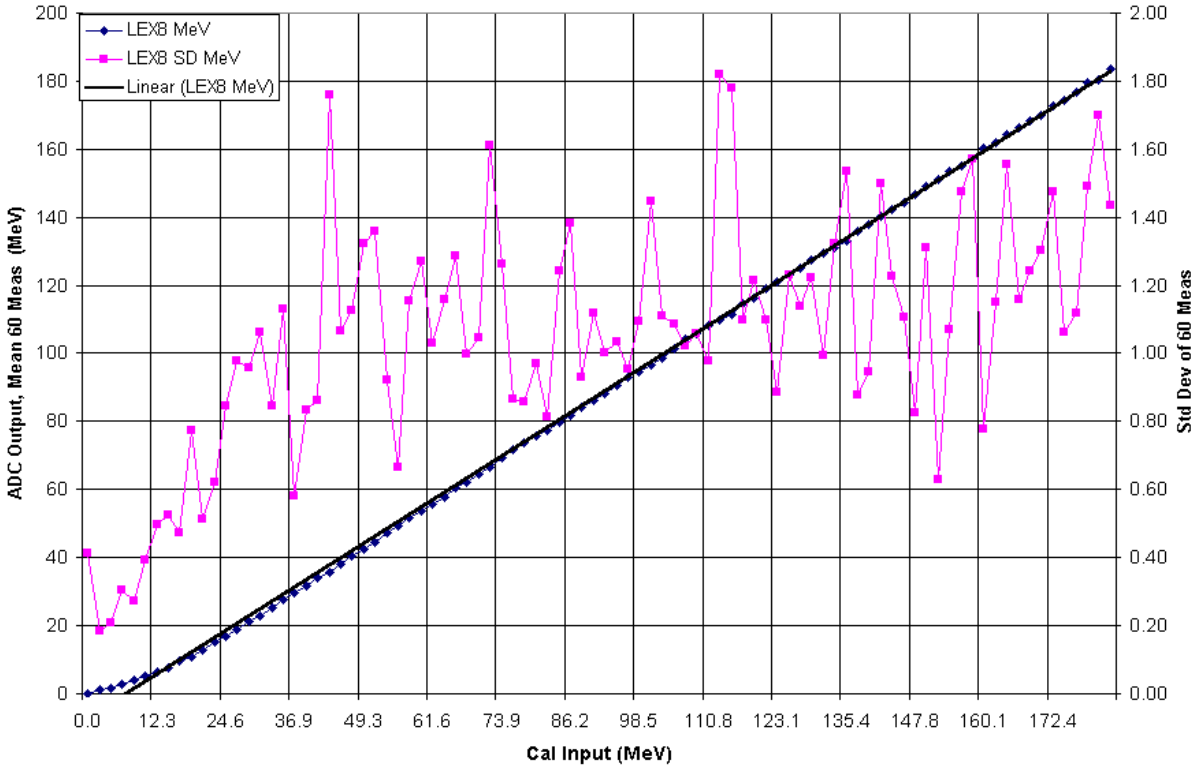


Figure 18: LEX1 Noise and Linearity Plot

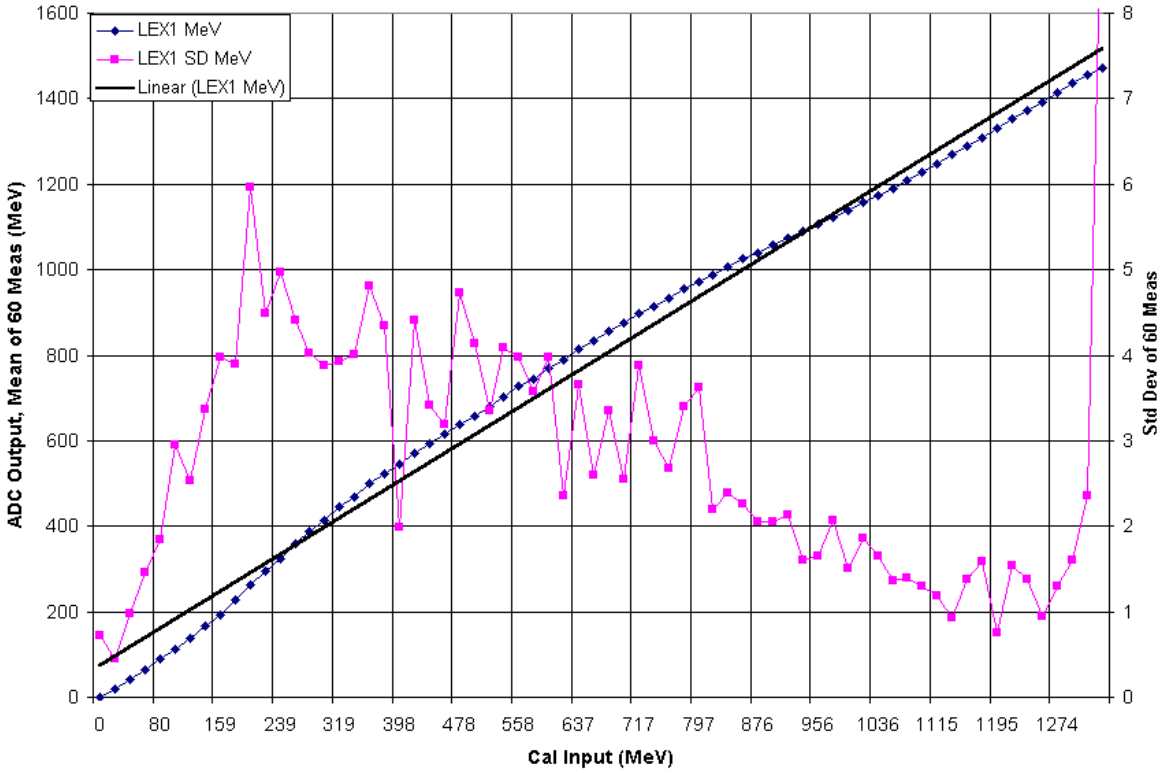


Figure 19: HEX8 Noise and Linearity Plot

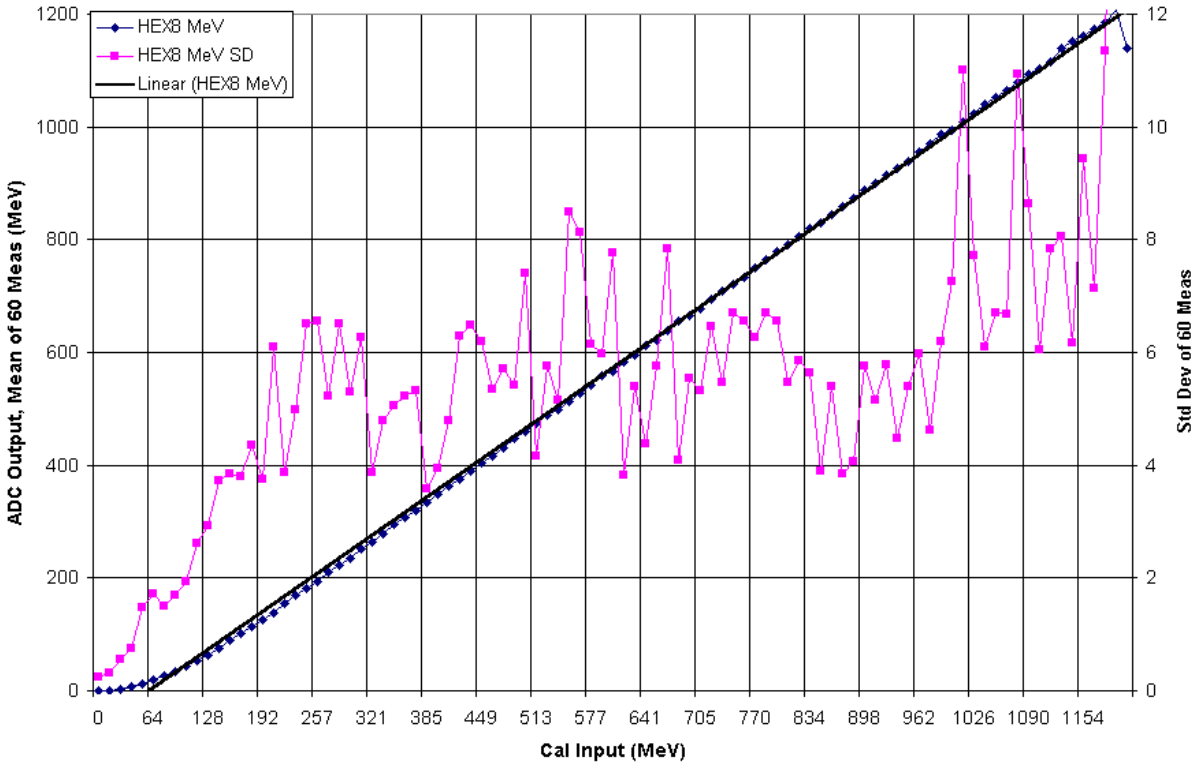


Figure 20: HEX1 Noise and Linearity Plot

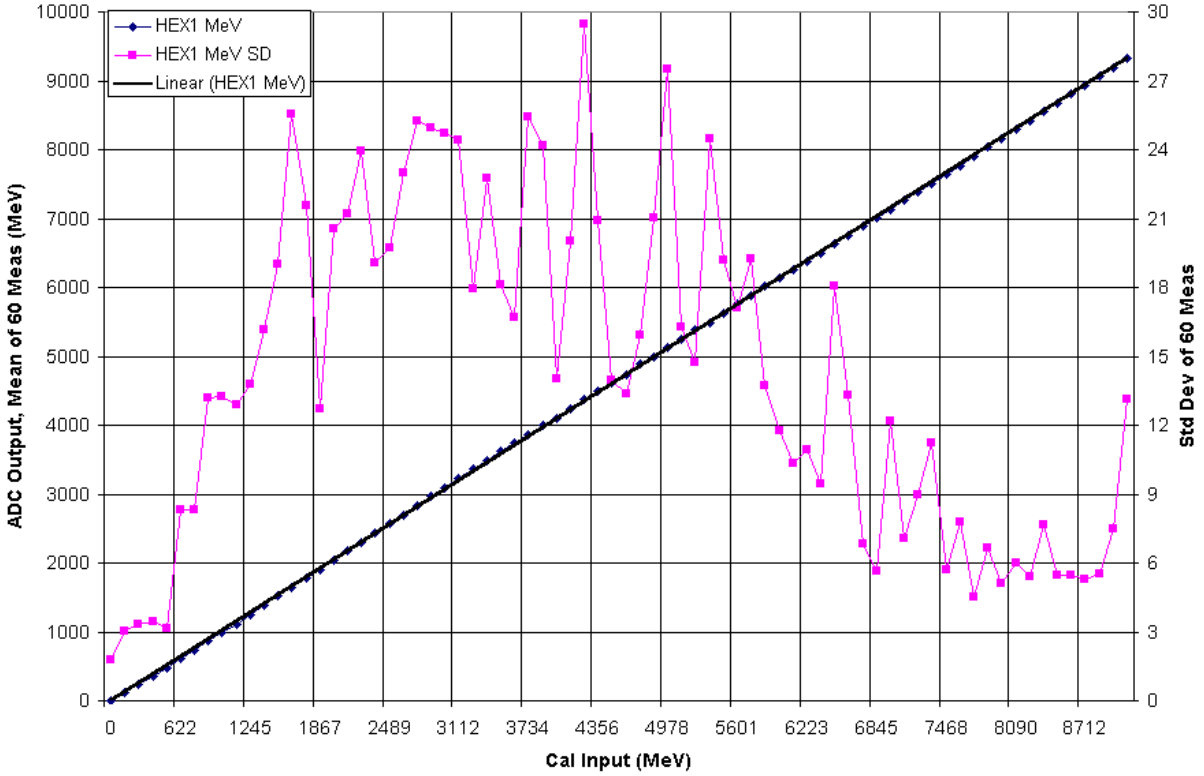
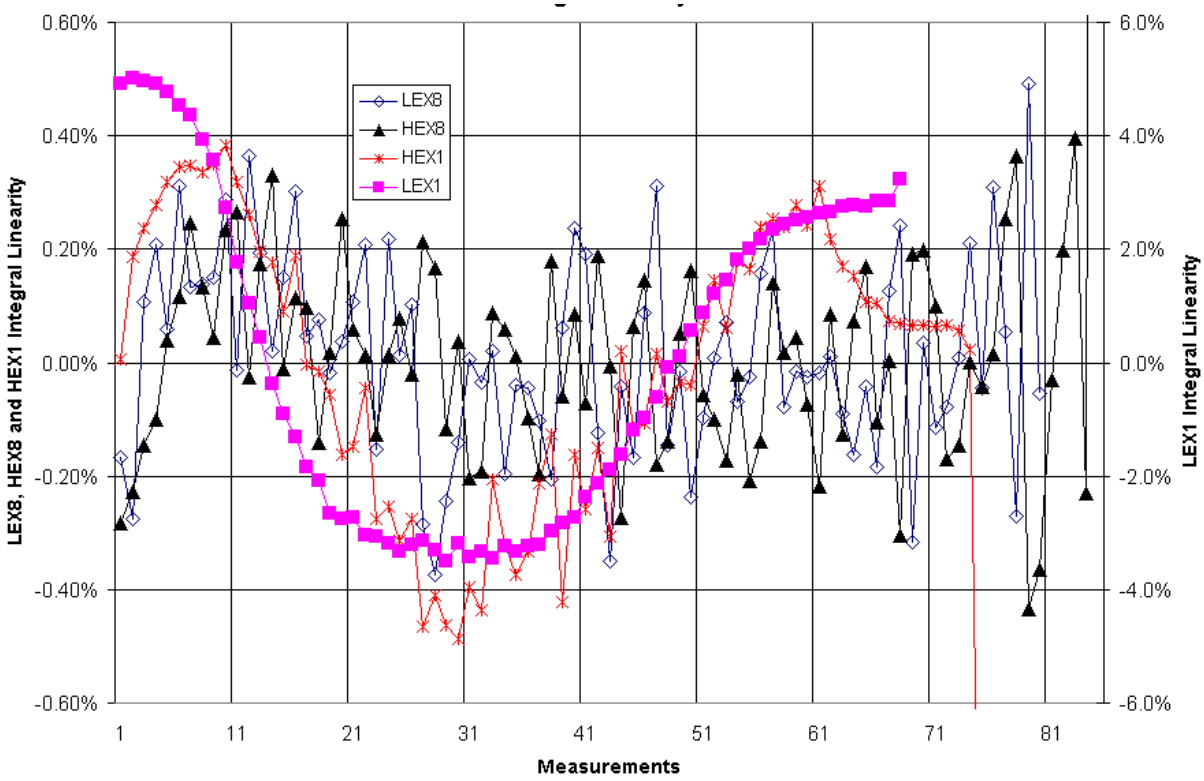


Figure 21: Integral Linearity Plot



Appendix A: Calculation from Volts to MeV for Calibration Pulse:

The capacitors on the test board for injecting an external pulse were measured:
Capacitance of C22 (LE) = 5.04 pF
Capacitance of C23 (HE) = 5.08 pF on test board S/N 1.

Full-scale measurements with an External pulse were measured to correlate with measurements from a calibration strobe source:

	External Source		Calibration Source		
	In	Out	In	Out	Cal Gain
LEX8	0.03	2.205	1.119	2.212	0
LEX1	0.19	2.119	0.73	2.112	1
HEX8	0.25	1.89	0.961	1.894	0
HEX1	0.25	0.346	0.109	0.358	1

From this data the capacitance of the Cal Gain 0 and Cal Gain 1 components was determined:

Cap(cal0) = (LEX8 Ext Input Volt / LEX8 Cal Input Volt) * LE External Capacitor Value
= (0.03 V / 1.119 V) * 5.04 pF
= 0.135 pF

Cap(cal1) = (LEX1 Ext Input Volt / LEX1 Cal Input Volt) * LE External Capacitor Value
= (0.19 V / 0.73 V) * 5.04 pF
= 1.31 pF

Note that the HE Ext Source was damaged during the time of this management was was not used as a double-check of these results.

Once the capacitance of the calibration pulse is known, the conversion from Volts to MeV was calculated as follows:

MeV = (Volts * Cap) / (Col/Elec * Elec/MeV)

Capacitance, Cal Gain = 0		1.35E-13 F
Capacitance, Cal Gain = 1		1.31E-12 F
Coulombs/Electrons		1.60E-19
Electrons/MeV	LE	5000
	HE	800

Volt to MeV Conversion (MeV/Volt) for Calibration Injected Pulse

LE Cal Gain=0	168.75
LE Cal Gain=1	1637.50
HE Cal Gain=0	1054.69
HE Cal Gain=1	10234.38